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09/843,650	04/27/2001	Shinji Ohuchi	IIZ 123	7849

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EXAMINER	
MITCHELL, JAMES M	
ART UNIT	PAPER NUMBER
2827	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/843,650	Applicant(s) OHUCHI	
	Examiner James Mitchell	Art Unit 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claims 1, 3, 4, 5, 6, 7, 11 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Anzai (US 6,323,551).

3. Anzai discloses a semiconductor apparatus comprising a semiconductor device (11d) to be mounted on a circuit board, a plurality of conductive post ("lead", 13) electrically connected to the semiconductor device and means for mounting the device onto a circuit board (Column 2, Line 1) by soldering (via solder contacts, 16), including a plurality of conductive bumps (16) respectively positioned on an outer end of each of the conductive post for soldering onto the circuit board, wherein a peripheral edge of resin (15) covering for sealing a surface of the semiconductor device and an outer edge of the conductive post (exposed surface) are inherently separated by a distance narrower than a height5 of the conductive post; wherein the semiconductor device is provided with a plurality of electrode pads (12) connected to the conductive posts with each pad arranged between two conductive post; with the conductive bumps of solder (Col.5,

Lines 6-7); the molding shaped to have a step (shown Fig 1A; via top molding, 15) along the entirety of a peripheral edge of the semiconductor device, the step having upper (top surface) and lower portion (portion below solder, 16); said molding resin not covering a peripheral side surface of each conductive post (Abstract) and an inherent insulating layer (via chip manufacture) formed on a peripheral surface of the semiconductor device between an upper surface of the semiconductor device and conductive post, wherein the molding resin is shaped to have a peripheral side surface on the identical plane with side surface of the semiconductor device; and peripheral side surface of each conductive post is formed in the same plane as that of the peripheral side surface of the semiconductor device.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anzai.

6. Anzai discloses the elements stated in paragraph 3, but does not appear to disclose that the difference in level between the upper portion and lower portion is half of a thickness of the mold resin between 40 and 60 micrometers, or that the insulating layer ahs a width of 100 to 200 micrometers.

7. In any case, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization for the difference in level between the upper portion and lower portion to be half of a thickness of the mold resin resin between 40 and 60 micrometers because applicant has not disclosed in the specification that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

8. Claims 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Anzai as applied to claim 11 and further in combination with Taguchi (U.S 6,285,085).

9. Anzai discloses that the first conductive bump is solder but does not appear to disclose a second conductive bump formed on the respective peripheral portion of the conductive post.

10. However Taguchi (Fig 1) utilizes a second conductive bump formed on the side surface of a conductive post.

11. It would have been obvious to one of ordinary skill in the art to incorporate a second conductive bump formed on the side surface of the conductive post of Anzai in order to provide for lateral mount (shown Taguchi Fig 14) and a connection surface to circuit substrates thereby reducing the area for connection as taught by Taguchi (Column 4, Lines 22-25).

12. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasunaga et al. (U.S 6,191,493).

13. Yasunaga (Fig 2, 3, 25, 33) discloses a semiconductor apparatus comprising a semiconductor device (3), a plurality of conductive posts (9) electrically connected to the semiconductor device, a plurality of conductive solder bumps (10) each provided on an outer end of the conductive posts, wherein a distance between a peripheral edge of the semiconductor device and an outer edge of the post is determined to be narrow; a plurality of pads (8) connected to the posts with the pads being arranged on a line extending the center of the semiconductor device; with a plurality of electrode pads being arranged between two adjacent conductive post wherein the pads connected to the post are arranged directly under a corresponding post (Fig 3); a molding resin (1) which covers a surface of the semiconductor device; and insulating layer (13) which is formed at portions corresponding to the conductive posts and at a peripheral portion of said semiconductor device, wherein the molding resin is on the identical plane with a peripheral side surface of the semiconductor device; and means for mounting device (Fig 35) onto a circuit board ("Col. 20, Lines 10-11) by soldering (53) conductive bumps (10) positioned on an outer end of conductive post (9).

14. With respect to claims 2, 8 and 9, Yasunaga does not appear to disclose the distance of the post to the edge of the device is in a range between 50 to 100 micrometers such that the distance is narrower than the height of the conductive post, the resin shaped to have a step having an upper and lower portion wherein the difference in level is half of a thickness of the mold resin, the lower portion of the step ranging between 40 to 60 micrometers, or the insulating layer having a width of 100 to 200 micrometers.

15. See paragraph 7.

Response to Arguments

16. Applicant's arguments with respect to claims 1-14 have been considered but are not found persuasive. Applicant tries to establish criticality of the placement of the conductive posts by indicating that the invention provides an advantage that bumps can be recognized visually, and has an ability to radiate heat; applicant fails to address the criticality of the step molding resin. However bumps being able to be recognized visually are not an unobvious purpose and don't produce an unexpected result. Furthermore, any array of bumps can be recognized visually and the ability to radiate heat is not exclusive to bumps being in the claimed position.

Allowable Subject Matter

17. Claims 15-22 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: The prior art does not disclose or make obvious removing a part of a molding resin over a wafer such that the resin is stepped shape at a peripheral edge or providing

a wafer with grooves at portions corresponding to dicing lines filled with insulating material while a part of a pad is not covered with a metal post in the groove and molding the wafer such that the resin is on the same plane as the post.

Conclusion

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Mitchell whose telephone number is (703) 305-0244. The examiner can normally be reached on M-F 10:30-8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703)

305-3432 for regular communications and (703) 305-3230 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jmm
January 1, 2003

DAVID E. GRAYBILL
PRIMARY EXAMINER